RATE COMPENSATING TRACKER WOX-2A

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RATE COMPENSATING TRACKER WOX-2A

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ABSTRACT: An automatic tracker was built to follow the position of the maximum of a correlation function generated by a DELTIC correlator. The position-correcting decisions, made for each successive correlogram, are of a fixed size (0.8 μsec); the direction is determined by the polarity of the error signal formed by comparing the tracker position with the position of the new correlogram. This is similar to the WOX-1A tracker, except that the WOX-2A is digital. Further, this tracker includes a rate tracking capability so that a correlogram whose position changes at a constant rate (up to 28.2 μsec/sec) may be tracked without lag. A direct readout of the correlogram rate of change of position is provided. Theoretical analysis shows that with such rate compensation the tracker performance approximates that of the uncompensated tracker for input standard deviations up to about 300 μsec, in addition to eliminating the lag. Beyond that, the tracker output variations increase and there is some tendency to oscillate.

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This report describes a "second generation" automatic tracker designed for use with the PUFFS system. The principal objective in this model was to eliminate the bearing lag caused by target bearing movement observed in the first model. This work was conducted under Task No. RUSD-4C150/212-1, "PUFFS Technical Direction". The present report will be of immediate interest to anyone concerned with the sonar tracking problem; in addition the principles and techniques involved should be of interest to anyone concerned with radio direction finding, navigation, or radar target tracking.

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Commander

Zolia I Slawsky

Z. I. SLAWSKY
By direction

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ILLUSTRATIONS

RATE COMPENSATING TRACKER WOX-2A

INTRODUCTION

1.1 An automatic tracker, reference (1), has been built to follow correlograms generated by a DELTIC correlator, reference (2). A tracking gate with a width appropriate to the correlogram width is split into two equal parts. The areas within each half are compared and an error signal is generated. The polarity of the error signal causes the gate to move a fixed amount, independent of the magnitude of the error, in the direction which will decrease the error. Incremental movements are made to correct the gate position as frequently as correlograms are generated by the DELTIC correlator.

1.2 When the input correlogram is moving, the tracking gate must lag the correlation maximum in order to make enough correct decisions to follow it. This lag depends upon the signal-to-noise ratio, the size of the fixed step, and the rate of change of position of the correlation maximum. This lag is considered to be serious enough to make it worthwhile to eliminate it.

1.3 Regardless of the signal-to-noise ratio or step size, there must be a rate of change of position (hereafter called a "rate") before there will be any lag. If the rate is measured and then compensated for, the tracker will follow without lag a correlogram whose delay time is changing at a constant rate. This report is a description of such a rate compensating tracker.

GENERAL THEORY OF OPERATION

2.1 The simplified block diagram in Figure 1 represents the general points of the design philosophy of the rate tracker.

2.2 The 2.46 mc input to the position changing logic comes from the DELTIC timing circuits and synchronizes the tracker with the DELTICS. The position changing logic controls changes in the tracking gate position. It is basically retiming circuitry that times the add and drop instructions from other parts of the tracker with a 1.23 mc pulse train going to the position memory. This memory is simply a 15 stage binary counter; with 1.23 mc in, the counter output is 37.6 cps, identical to the

DELTIC transfer pulse frequency. Adding or dropping pulses from the input to the memory merely changes the phase of the 37.6 cps out with respect to the transfer pulses.

2.3 The tracking gates consist of a left gate and a right gate, each of equal duration and with essentially no time between them. They are generated from the output of the position memory, so their position relative to the transfer pulse changes with the 37.6 cps output. To move the gates left one step, a single pulse is added to the 1.23 mc; to move right, a pulse is dropped.

2.4 Previous models of the tracker measured the area of the correlogram within the tracking gates by analog methods. However, the DELTIC correlator actually compares the pulse trains in the DELTICS for agreements and disagreements at a 9.84 mc rate, and the resulting pulses must be smoothed to obtain the analog correlation function. The number of agreements in an interval of time is proportional to the area of the correlation function for that time interval, and no conversion to analog form is necessary for measuring areas. The difference in the number of agreements occurring in two consecutive periods of time, say the left and right gates, is proportional to the difference in areas within the gates. If A is the number of agreements and A' the number of disagreements occurring in the left gate, then $A + A' = T_g$, the number of comparisons occurring in the gate length. Similarly, if B and B' represent the agreements and disagreements respectively in the right gate, then $B + B' = T_g$. If $A - B > 0$, there is more "area" in the left gate and we want a decision* to move left one step. However, $A - B = A - T_g + B'$, and the requirement that $A + B' > T_g$ is equivalent to requiring that $A - B > 0$ for a left decision. A resettable counter T_g units long can be built to count $A + B'$; overflow from this counter (the decision element) constitutes a decision to move left, and no overflow means move right. When $A + B' = T_g$, the gate moves left. The effect of this arbitrary decision is explained in the theoretical discussion.

2.5 The system as described so far is a digital version of Target Tracker WOX-1A. It is capable of tracking a correlogram with a changing position, but it tracks with a lag. The remainder of the system compensates for the rate-of-change of

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* The use of the word "decision" in this report refers only to the instruction from the decision element to move the tracking gate left or right.

correlogram position, which can be estimated by comparing the number of left and right decisions, and eliminates the lag when the rate is constant.

2.6 The rate memory is a ten stage reversible binary counter whose last five stages gate five pulse frequencies with a binary relation, the largest of which is 37.6 pps and the smallest 2.4 pps. Thus, depending on the binary number stored in the rate memory, drop pulses may be fed to the position changing logic at frequencies ranging from 0 to 72.9 pps in increments of 2.4 pps. These pulses will then move the gate position at a constant rate related to the binary count in the rate memory.

2.7 If the correlogram is moving to the right at a rate larger than the estimate stored in the rate memory, more right decisions will occur than left decisions when the correlogram is being tracked. Each right decision increases the count in the rate memory by one, and each left decision subtracts one count from the stored rate estimate. Thus the excess of right decisions will increase the number stored in the rate memory until it equals the actual correlogram bearing rate. Similarly if the estimate in the rate memory is too high, more left decisions will result and the count will be decreased. Once the rate estimate stored in the rate memory becomes equal to the actual correlogram rate and the lag reduces to zero, left and right decisions will be made with equal probability and there will be no further tendency for the stored rate estimate to change. Since the rate estimate is made up of the difference between the number of left and right decisions made by the tracker and since the rate will be compensated for some finite value of this difference, the frequency of left and right decisions must eventually become equal and the lag for any constant rate will become identically zero.

2.8 By constantly adding 37.6 pps to the 1.23 mc into the position counter we can control a net range of add or drop frequencies from 37.6 pps added to 35.2 pps dropped in increments of 2.4 pps. Thus we can compensate for rates up to 30.1 μsec/sec to the left and up to 28.2 μsec/sec to the right.

DESCRIPTION OF OPERATION

3.1 This section is essentially a verbal description of the block diagram shown in Figure 2.

3.2 The 2.46 mc clock pulses from the DELTIC timing circuits trigger a flip-flop. The transistor collectors change state at 1.23 mc and are 180° out of phase. One phase, call it

the α phase, generates the pulses which are normally passed to the position counter. The β phase is normally not passed to the position counter but permits adding pulses that occur between those from the α phase.

3.3 The α phase resets the "drop flip-flop" whose output keeps a gate open as long as it is in the reset state. This gate passes the 1.23 mc α phase through an "or" gate into the position counter. A drop input pulse sets the drop flip-flop, thereby closing the gate for one of the 1.23 mc α phase pulses. All stages of the position counter then must wait 0.8 μsec longer before changing state.

3.4 A decision to move left sets the "decision flip-flop". A reset pulse, formed by a change from - to + in the position counter output stage, causes this flip-flop to revert to its original state, thereby generating a pulse that sets the "add-two" flip-flop. The next 1.23 mc β phase pulse resets it, thereby adding one pulse to the position counter and also setting the "add-one" flip-flop. The second 1.23 mc β phase pulse resets this flip-flop and a second pulse is added to the position counter. In this manner two extra pulses are added to the position counter for each decision to move left, which has the effect of moving the gate two steps left. A decision to move right moves the gate not at all. This corresponds to a movement left of one step for a left decision or a movement right of one step for a right decision, superimposed upon a constant movement of one step left each decision. This constant one step left per decision is necessary for the rate compensation feature of the tracker as mentioned earlier.

3.5 An input to the "add-one" flip-flop through the "external add" or "slow left" will add one pulse to the position counter. Figure 3 shows photos of the 1.23 mc from the "or" gate.

3.6 The position counter has 15 binary stages and divides the 1.23 mc to 37.6 cps, the frequency of the DELTIC transfer pulses. The effect of the add and drop gates in the position changing logic just described is to change the phase of the 37.6 cps "advance pulse" from the position counter relative to the transfer pulse.

3.7 The tracking gates are generated by the position counter. The "pre-gate flip-flop" is set by the advance pulse. For a gate width of 52 μsec, this flip-flop is reset by the 19.2 kcps output. This causes the left gate flip-flop to set; it is reset by the 19.2 kcps also. Resetting the left gate flip-flop sets the right gate flip-flop, which is similarly reset. Thus the two gates are precisely timed by the 19.2 kcps

signal so they are of identical duration and essentially no time exists between them. Gate widths of 52, 104, 208 and 416 μsec are desired, so a gate width switch for selecting the 19.2, 9.6, 4.8 or 2.4 kcps output of the counter is mounted on the front panel.

3.8 The pulse for resetting the decision counter and triggering the rate counter is formed by the "reset flip-flop" following the right gate flip-flop, operating in exactly the same manner in which the gates are formed. Figure 4 shows the time relationship of the gates and pulses.

3.9 For a 52 μsec gate width, the gate length T_g equals 512 possible agreements and disagreements and the decision counter must be ten stages long. A change of state in the tenth stage indicates overflow and sets the decision flip-flop. Having a variable gate width means the counter length must be variable, and another switch is ganged with the gate width switch to select the appropriate overflow stage. For the 416 μsec gate, T_g equals 4096 counts and the thirteenth stage is tapped.

3.10 Provision is made for controlling the gate position by means of externally generated decisions by placing a decision selection switch in the line from the output of the decision counter. Another switch in this line lets the operator insert add or drop decisions constantly. This enables him to make small adjustments in the gate position or to preset the rate counter.

3.11 The measure of uncompensated bearing rate is made by observing the excess decisions made in one direction over those made in the other direction. Decisions to move right are added and decisions to move left are subtracted in a reversible binary counter. The state of the decision flip-flop at the time it is reset represents the decision; therefore this flip-flop controls the add and subtract control buses in the counter. The reset pulse is added or subtracted depending on the level of the respective control buses.

3.12 The reversible counter is ten stages long. The most significant five control five gates; the gate on the most significant stage controls a constant 37.6 pps, the next most significant stage controls 18.8 pps and so on. The outputs of the gates are added. The advance pulse triggers a four stage divider to generate the drop frequencies. If changes from plus to minus are used to trigger the successive stages of this

divider, and changes from minus to plus are used to generate the gated drop pulses, none of the drop pulses will be superimposed even when all the gates are open. Figure 5 demonstrates this.

3.13 Since a pulse added or dropped from the 1.23 mc changes the tracking gate position 0.8 μsec, a drop frequency of 37.6 pps corresponds to a rate of change of position of 30 μsec/sec. The rate counter controls drop frequencies over the range 0 to 72.9 pps. However, 37.6 pps are added constantly, and the net range is from 37.6 pps added to 35.2 pps dropped. This means rates may be compensated from 30 μsec/sec to the left to 28.2 μsec/sec to the right in increments of 1.9 μsec/sec.

3.14 To operate the tracker without rate correction, the reset pulse can be interrupted by setting the "Rate Track" switch to "Off". Then the "Rate Reset" button must be operated to set the last five states so only the 37.6 pps gate is open; this will then compensate for the extra add pulse every decision. These controls are on the front panel.

3.15 Figures 6, 7, 8, and 9 show the circuit diagrams of the position counter, position changing logic with gate generators, decision counter, and rate counter with drop pulse generator, respectively. Figure 10 shows the interconnecting and front panel wiring. Figures 11, 12, 13, and 14 show photographs of the plug-in cards in the order mentioned above. Figure 15 is a photograph of the DELTIC and tracker rack with the front panel.

POWER REQUIREMENTS

4.1 The tracker uses the following supply voltages:

-4.5 volts @ 430 ma
+1.5 volts @ 11 ma

THEORETICAL PERFORMANCE OF TRACKER

5.1 The response of the tracker to a correlogram with a given standard deviation (σ_1) around its mean position and a given rate of motion (ρ) of its mean may be determined from equations derived in reference (3). The tracker parameters which are necessary for these equations are the position step size Δ, the rate step size θ, and the period between decisions T.

5.2 The 1.23 mc pulse rate into the position counter determines the step size as approximately 0.8 microseconds, and

the decision period is 0.026 seconds. Thirty-two net decisions in one direction are required to change the state of the rate counter stage which controls the lowest frequency or 2.4 pps input to the drop circuit. This 2.4 pps frequency represents a rate of (0.8)(2.4) or 1.9 μsec/sec. Thus the effective rate step size θ is $\frac{1.9}{32}$ or 0.06 μsec/sec for one rate decision, although the smallest step actually taken is 32 times this.

5.3 Thus we have the tracker parameters as T = 0.026 sec, Δ = 0.8 μsec and θ = 0.06 μsec/sec.

5.4 The effective smoothing time constant of the tracker is given by equation (12) of reference (3) as

$$\tau = \sqrt{\frac{\pi}{2}}\ \frac{\sigma_i}{\Delta}\ T = \sqrt{\frac{\pi}{2}}\ \frac{0.026}{0.8}\ \sigma_i = 0.0407\ \sigma_i$$

where τ is in seconds and σ_i is in microseconds. The standard deviation of the output position is given by equation (6) as

$$\sigma_o = \sqrt[4]{\frac{\pi}{8}}\ \sqrt{\Delta}\ \sqrt{\sigma_i} = \sqrt[4]{\frac{\pi}{8}}\ \sqrt{0.8}\ \sqrt{\sigma_i} = 0.708\ \sqrt{\sigma_i}$$

where both σ_i and σ_o are given in microseconds. With no rate compensation the lag due to an input rate will be given by

$$l = \sqrt{\frac{\pi}{2}}\ \frac{\rho}{\Delta}\ \sigma_i\ T = \sqrt{\frac{\pi}{2}}\ \frac{0.026}{0.8}\ \sigma_i\ \rho = 0.0407\ \sigma_i\ \rho$$

where l and σ_i are in microseconds and ρ is in μsec/sec.

5.5 With rate compensation, the average lag will be zero. However if the actual rate is not an integral multiple of 1.9 μsec/sec, the rate circuits must alternate between two states to make the average rate estimate equal to the actual rate. Thus the estimated rate will always differ from the actual rate, and the average magnitude of the error in rate compensation (averaged over time for a given actual rate, and over all rates) will be B/3 where B is the smallest step used in the rate compensation (B = 1.9 μsec). If this mean absolute rate compensation error is substituted into the lag formula, an expression is obtained for the mean absolute value (L) of the lag:

$$L = \sqrt{\frac{\pi}{2}}\ \frac{B}{3\Delta}\ \sigma_i T = \sqrt{\frac{\pi}{2}}\ \frac{1.9}{3(0.3)}\ 0.026\ \sigma_i = 0.026\ \sigma_i$$

where L and σ_i are in microseconds.

This mean absolute lag shows up in the output of the tracker as a variation of output position about its mean value, although the average lag is zero. It is not related to the statistical variation of the output (σ_o) due to input noise, but is caused by the coarseness of the rate steps. Because of the different dependence on σ_i this effect will be smaller than σ_o for small input standard deviations but becomes larger than σ_o for input standard deviations larger than about 750 μsec.

5.6 Another effect the rate tracking has is to produce a tendency toward oscillation of the tracker output about its mean value. This effect is shown by the denominator of the transfer function shown in equation (10) of reference (3).

$$H(s) = \frac{\Delta s + \theta}{\sqrt{\frac{\pi}{2}}\ \sigma_i\ Ts^2 + \Delta s + \theta}$$

The response is overdamped for small values of σ_i and is only oscillatory for large input standard deviations. The value of σ_i for which the system has a damping factor of one-half (slightly oscillatory) is:

$$\sigma_i = \sqrt{\frac{2}{\pi}}\ \frac{\Delta^2}{\theta T} = \sqrt{\frac{2}{\pi}}\ \frac{(0.8)^2}{0.06\ 0.026} = 328\ \mu\text{sec}$$

For input standard deviations smaller than this value the output will be well damped, but for larger input standard deviations there will be a definite tendency for the output to oscillate around its final value when disturbed. This oscillation is caused by the dynamic characteristics of the feedback in the tracker, and depends on the values chosen for Δ and θ. It is not in any way related to the mean absolute lag which was produced by the coarseness of the bearing rate corrections.

5.7 A bias error is introduced in this tracker due to the arbitrary decision made in the no-error case. If the number of agreements in the left gate exactly equals the number in the right gate, the tracker treats this as though the left gate contained a larger number and moves left. Thus the probability of moving left is increased slightly over that of moving right, and the tracker must move off the correlogram center to compensate for it.

5.8 For small signal-to-noise ratios the probability of occurrence of each agreement (or disagreement) pulse approaches $\frac{1}{2}$, so the number of pulses into the decision counter in each cycle is binomially distributed with $p = q = \frac{1}{2}$ and n equals the number of 9.84 mc pulse periods during which the two gates are on. The mean of this distribution is $\frac{n}{2}$ and the probability of exactly $\frac{n}{2}$ counts is approximately $\sqrt{\frac{2}{n\pi}}$. This is the probability of a false decision to move left and may be represented by an effective rate of $\sqrt{\frac{2}{n\pi}}\ \frac{\Delta}{T}$ μsec/sec.

5.9 Using this as ρ in the equation for lag gives the lag due to bias in the decisions as

$$\ell_b = \sqrt{\frac{\pi}{2}}\ \frac{\sigma_1}{\Delta}\ T\ \left(\sqrt{\frac{2}{n\pi}}\ \frac{\Delta}{T}\right) = \frac{\sigma_1}{\sqrt{n}}$$

For example, in the 104 μsec gate width position n = 2048 and $\ell_b = 0.022\ \sigma_1$ microseconds. Although this is a lag due to an effective rate, it is not possible to eliminate it by rate tracking. This is due to the point in the system (namely the decision element) where the error is introduced. Thus the bias ℓ_b will be present whether or not rate tracking is used.

5.10 Since ℓ_b is approximately the same magnitude as L, it will be small compared to the output standard deviation for σ_1 less than about 750 μsec. However, it differs from σ_o and L in that it is a definite bias whereas the other output variations have zero mean, thus no amount of additional smoothing will remove it from the mean gate position. It is felt that the magnitude of the effect is sufficient to be worth noting, but not intolerably large.

5.11 The conclusion of this analysis is that the rate tracker performance should approximate that of the tracker without rate correction for input standard deviations less than about 300 μsec, except for the elimination of lag. When the standard deviation of the input is larger than 300 μsec, rate correction will be accompanied by increased output variation and a tendency to oscillate about the mean due to both of the above-mentioned causes. However, tracking can probably still be accomplished up to an input standard deviation of about 1000μsec, at which point the rms output noise becomes an appreciable part of the gate width and the probability of the gates wandering completely off the target is non-negligible.

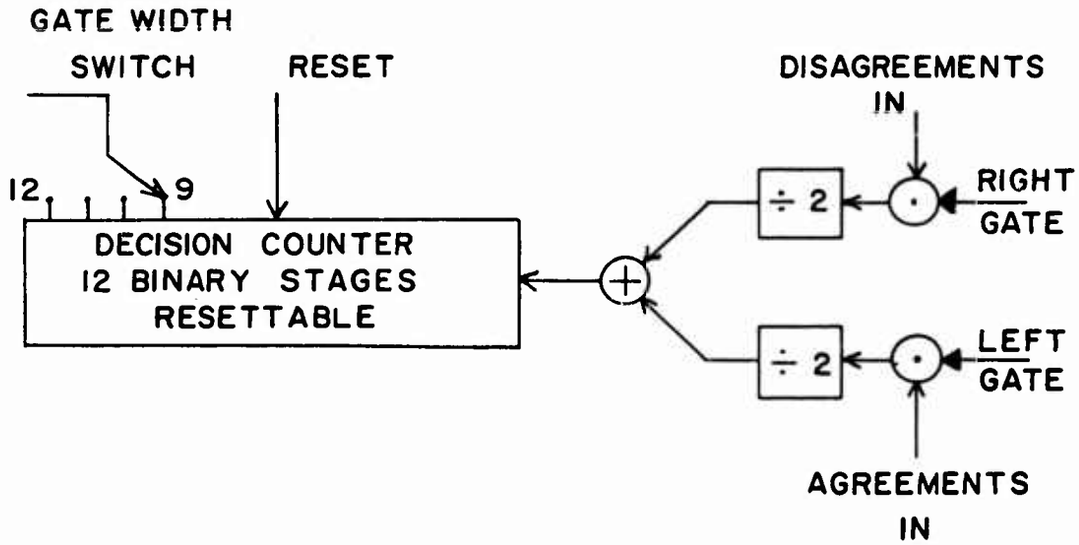
ADDENDUM

The bias error discussed in sections 5.7 through 5.10 may be eliminated by a change in the decision counter and its gating logic. The bias is generated by the arbitrary decision to move left when the number of agreements in the left gate exactly equals that in the right gate (i.e., when the number of agreements in the left gate plus the number of disagreements in the right gate equals T_g). This bias can be eliminated either by producing a zero decision (no motion of the gates) in the "equal-area" case, or by letting the gates move either alternately or statistically in either direction with equal relative frequency when the equal-area case occurs.

The modification shown below accomplishes this, making a statistical decision to move one way or the other each time the equal-area case occurs. The binary divide-by-two stages are wired so that they produce an output pulse for each even-numbered input pulse after they are reset. Thus the number of output pulses from the binary stage during a gate is n/2 if the number of input pulses, n, is even; and is (n-1)/2 if n is odd.

In the special case where the total number of input pulses is equal to T_g (T_g is always an even number), two possible conditions may occur. Either A and B' (number of agreements in left gate and number of disagreements in right gate respectively) are both even or they are both odd. If they are both even, the total number of pulses into the decision counter will be $A/2 + B'/2$ or $(A + B')/2$. If they are both odd, the total number into the decision counter is $(A-1)/2$ plus $(B'-1)/2$ or $\left[(A + B')/2\right] - 1$. Thus if the decision counter is shortened by one stage, it will overflow in the first case and not in the second; when in each case $A + B'$ equals T_g. It may be readily verified that the shortened decision counter will overflow whenever $A + B'$ is greater than T_g and will not overflow when $A + B'$ is less than T_g. It is also evident that A and B' have equal probabilities of being even or odd, due to the smoothness of the binomial distribution. Therefore the tracker will move left or right in the equal-area case with equal probability, and the bias due to this problem will be eliminated.

This modification was not developed in time to be incorporated in the WOX-2A Tracker, but it will be used in later trackers to eliminate the problems associated with the arbitrary left decision.



Decision Counter and Gating Logic as Modified

See Figure 2

REFERENCES

(1) J. C. Munson, G. W. Cope, A. H. Sabelhaus, "Target Tracker WOX-1A", NAVORD Report 6799.

(2) J. C. Munson and L. E. Barton, "Delay Line Time Compressor WOX-3A", NOLTR 61-47 (In preparation).

(3) C. N. Pryor, "Analysis of the Puffs Tracker WOX-1A as a General Nonlinear Filter", NAVWEPS Report 7375.

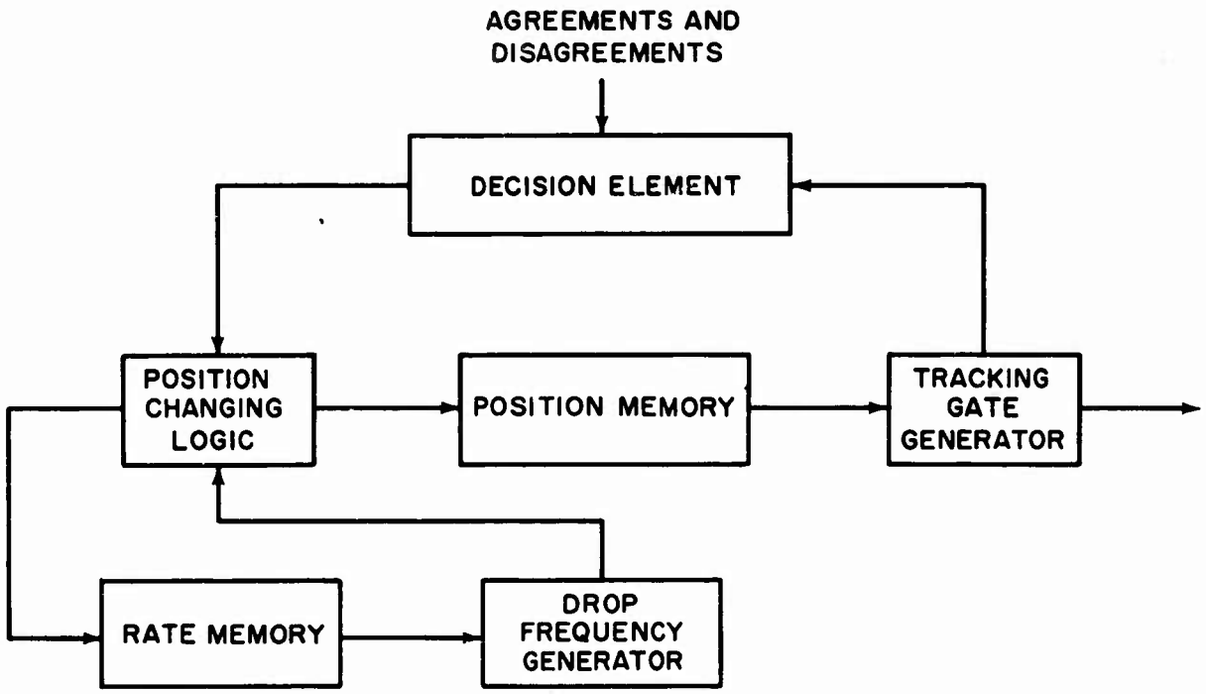


FIG. I ESSENTIAL BLOCK DIAGRAM OF RATE TRACKER

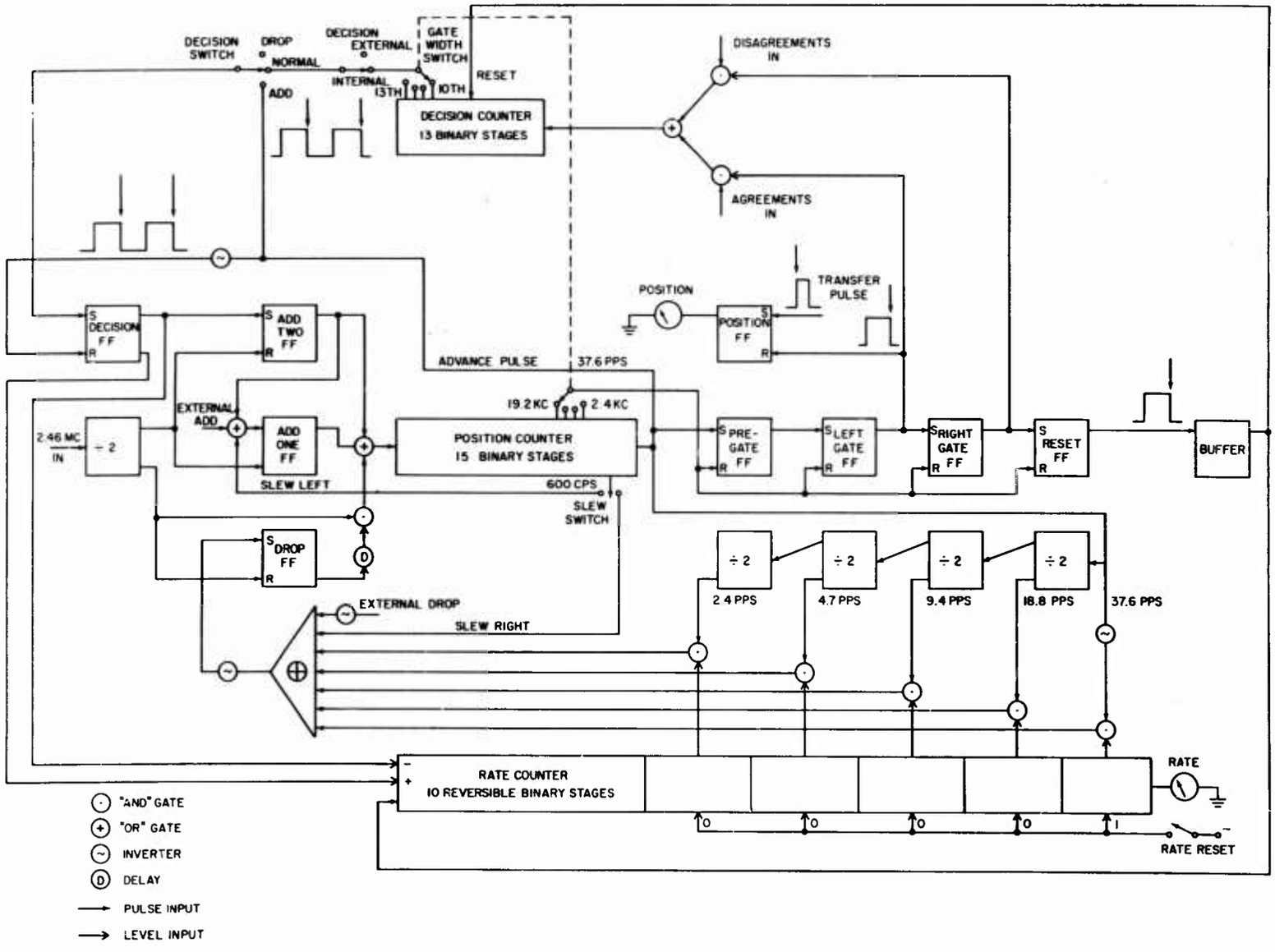
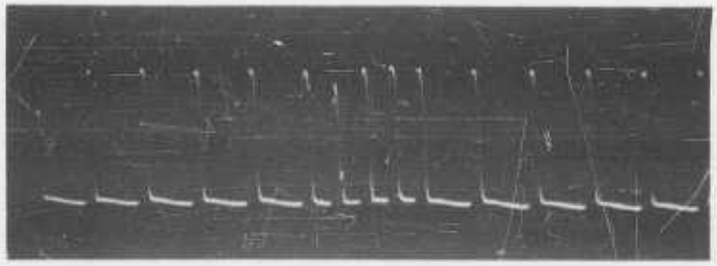


FIG. 2 DETAILED BLOCK DIAGRAM OF RATE TRACKER

(a) ONE PULSE DROPPED

(b) ONE PULSE ADDED



(c) TWO PULSES ADDED

FIG. 3 PHOTOGRAPHS OF 1.23 MC INTO POSITION COUNTER

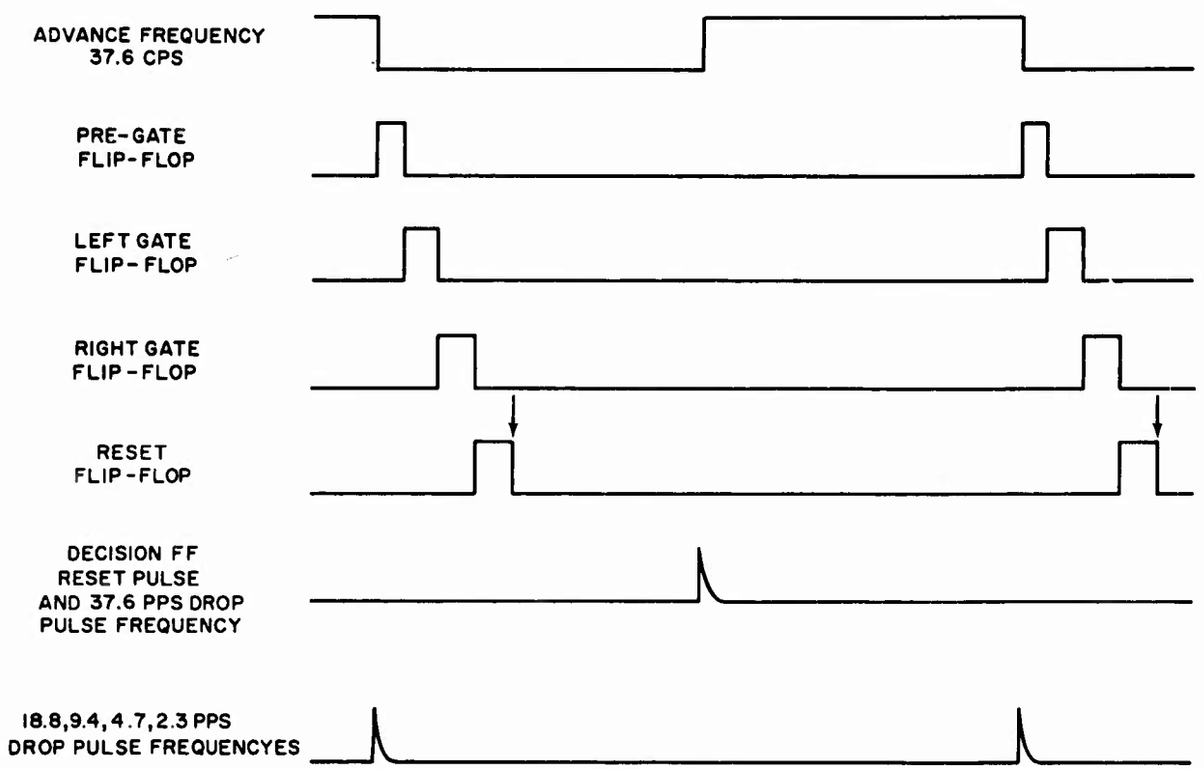


FIG. 4 TRACKING GATE AND PULSE TIMING WAVEFORMS

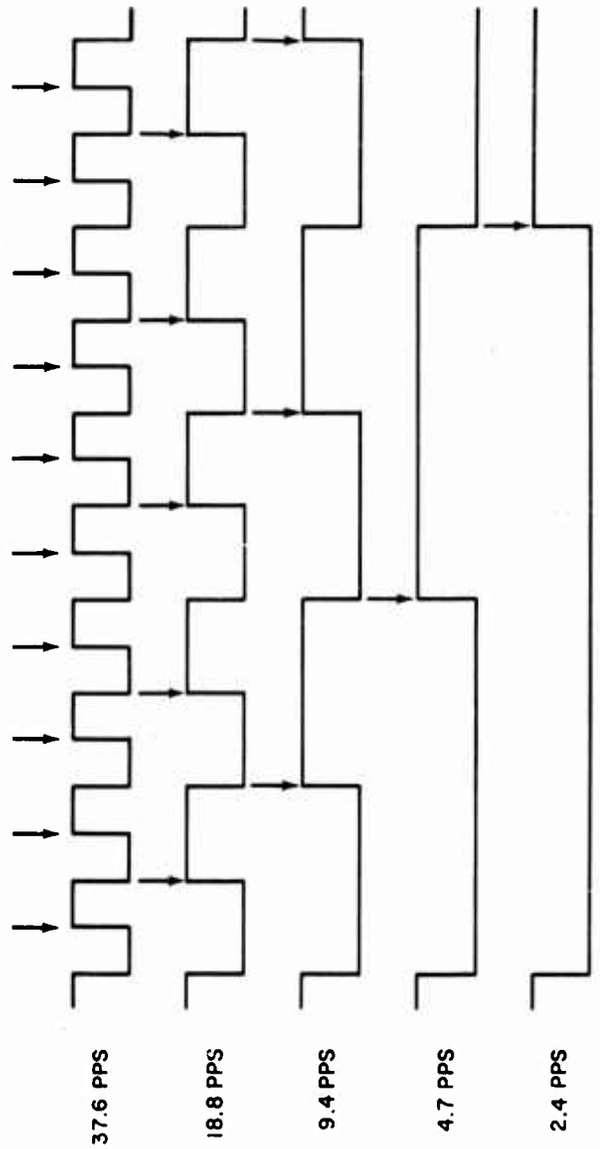


FIG. 5 DROP PULSE FREQUENCY GENERATOR WAVEFORMS

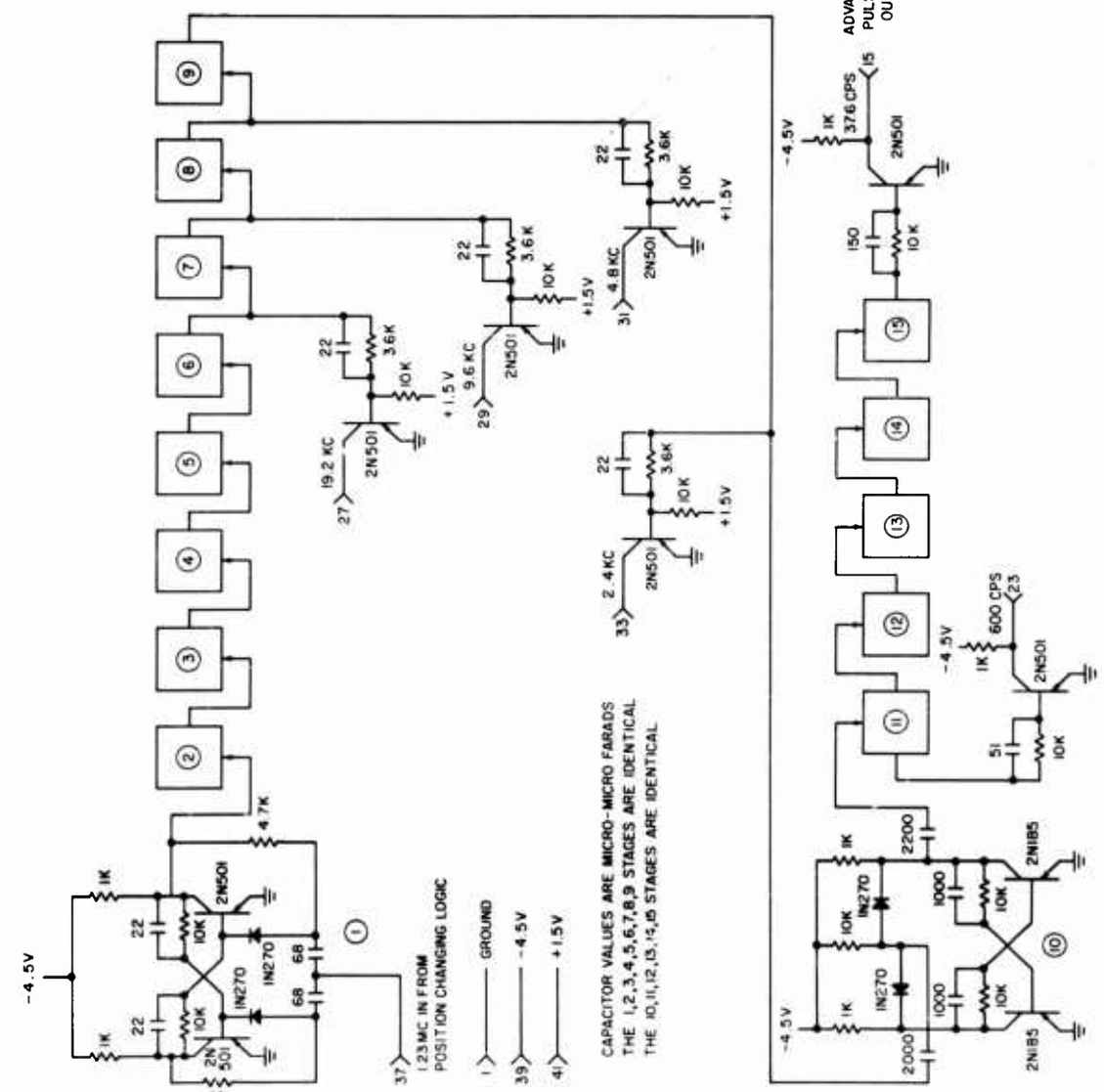


FIG. 6 POSITION COUNTER CIRCUIT DIAGRAM

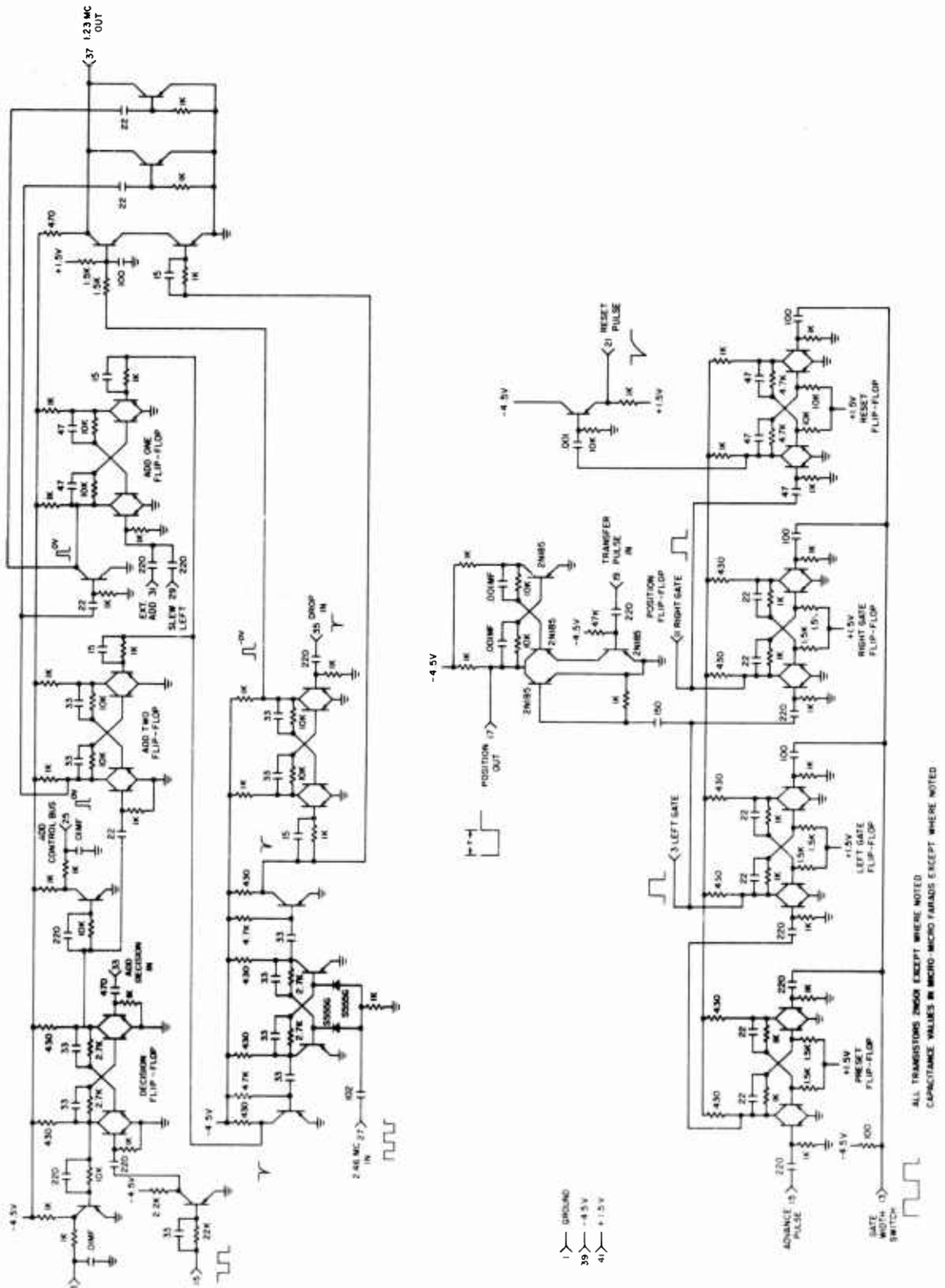


FIG. 7 POSITION CHANGING LOGIC AND GATE GENERATOR CIRCUIT DIAGRAM

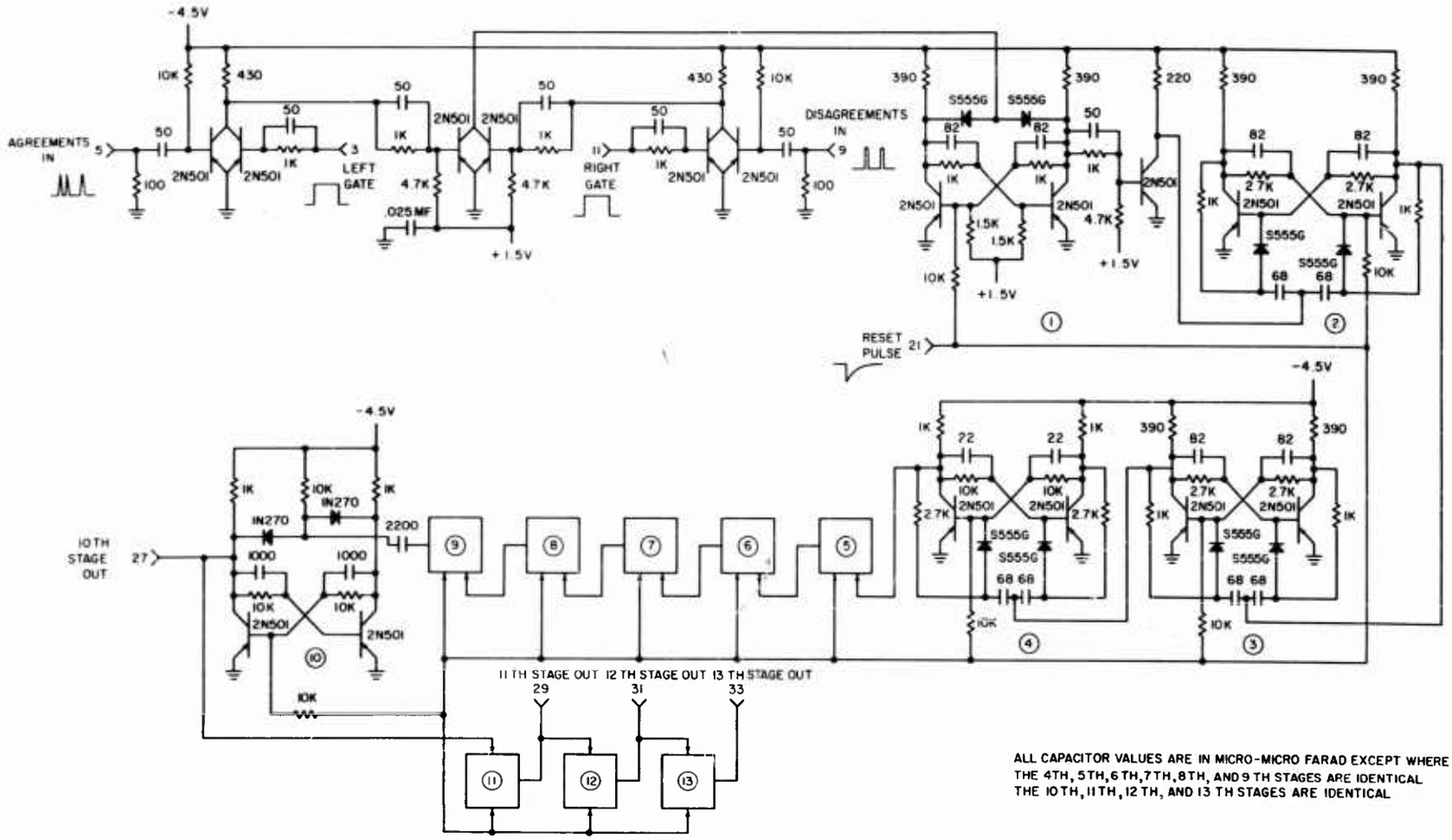


FIG. 8 DECISION COUNTER CIRCUIT DIAGRAM

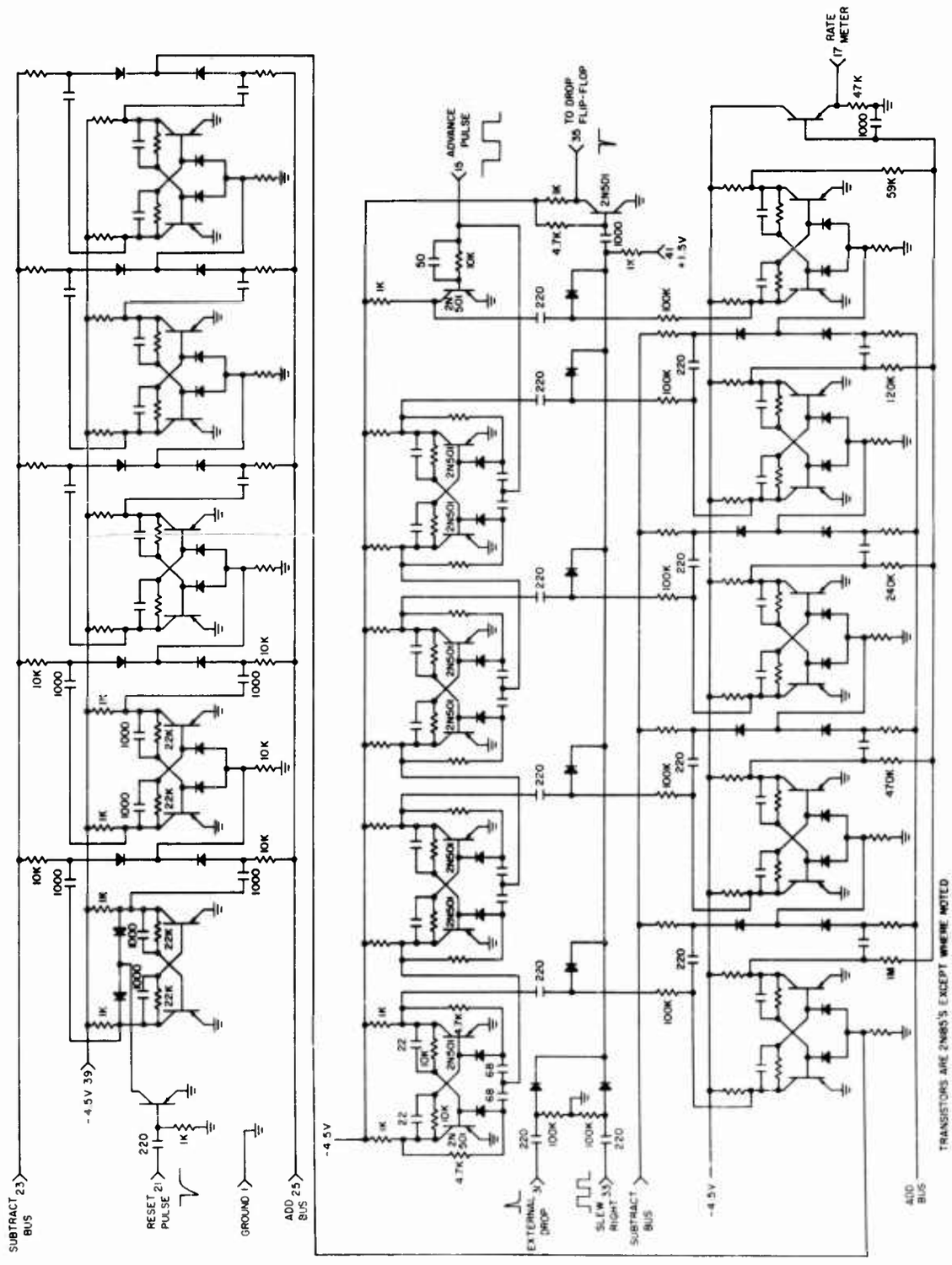


FIG. 9 RATE COUNTER AND DROP FREQUENCY GENERATOR CIRCUIT DIAGRAM

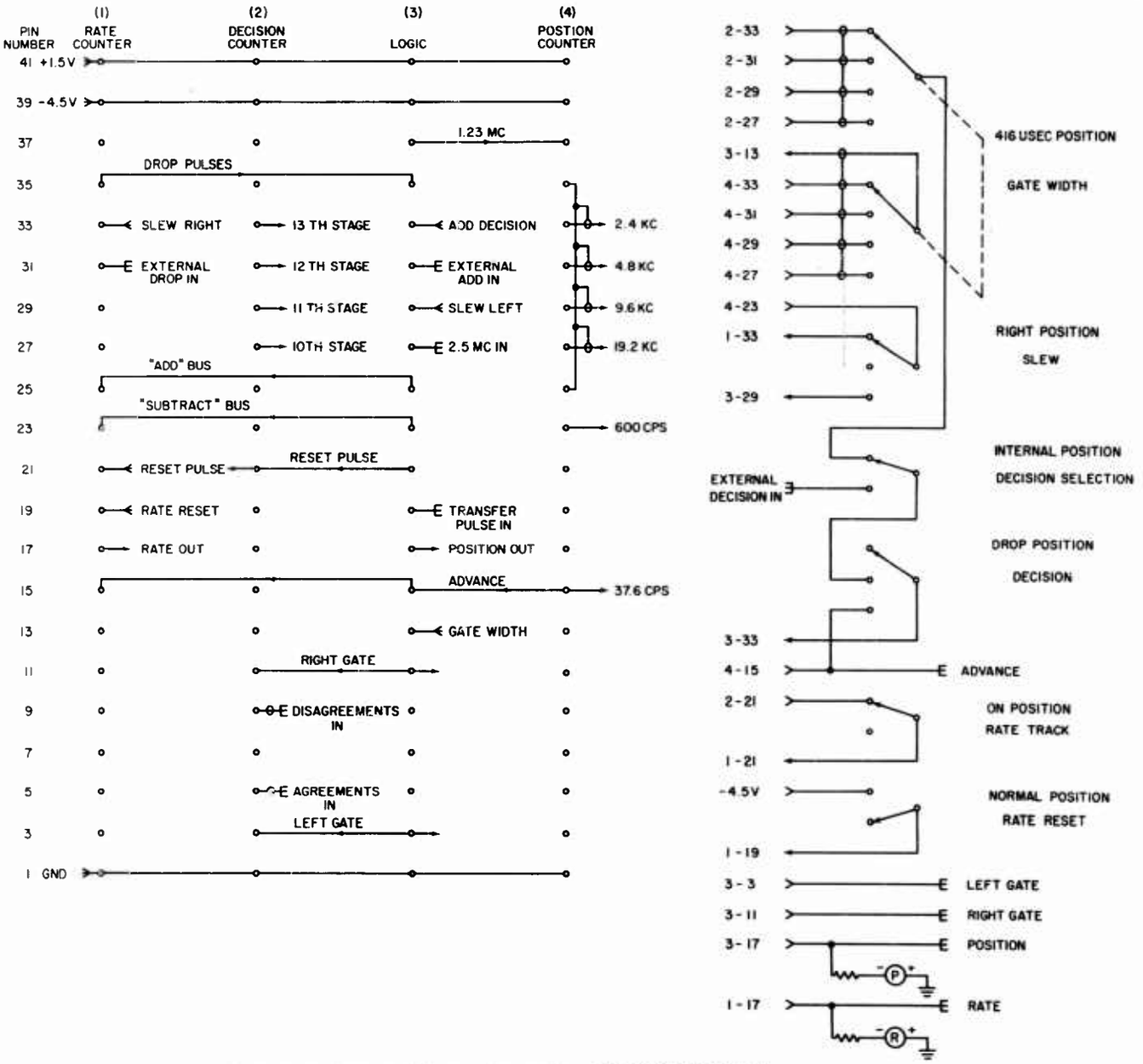


FIG. 10 CHASSIS AND FRONT PANEL WIRING DIAGRAM

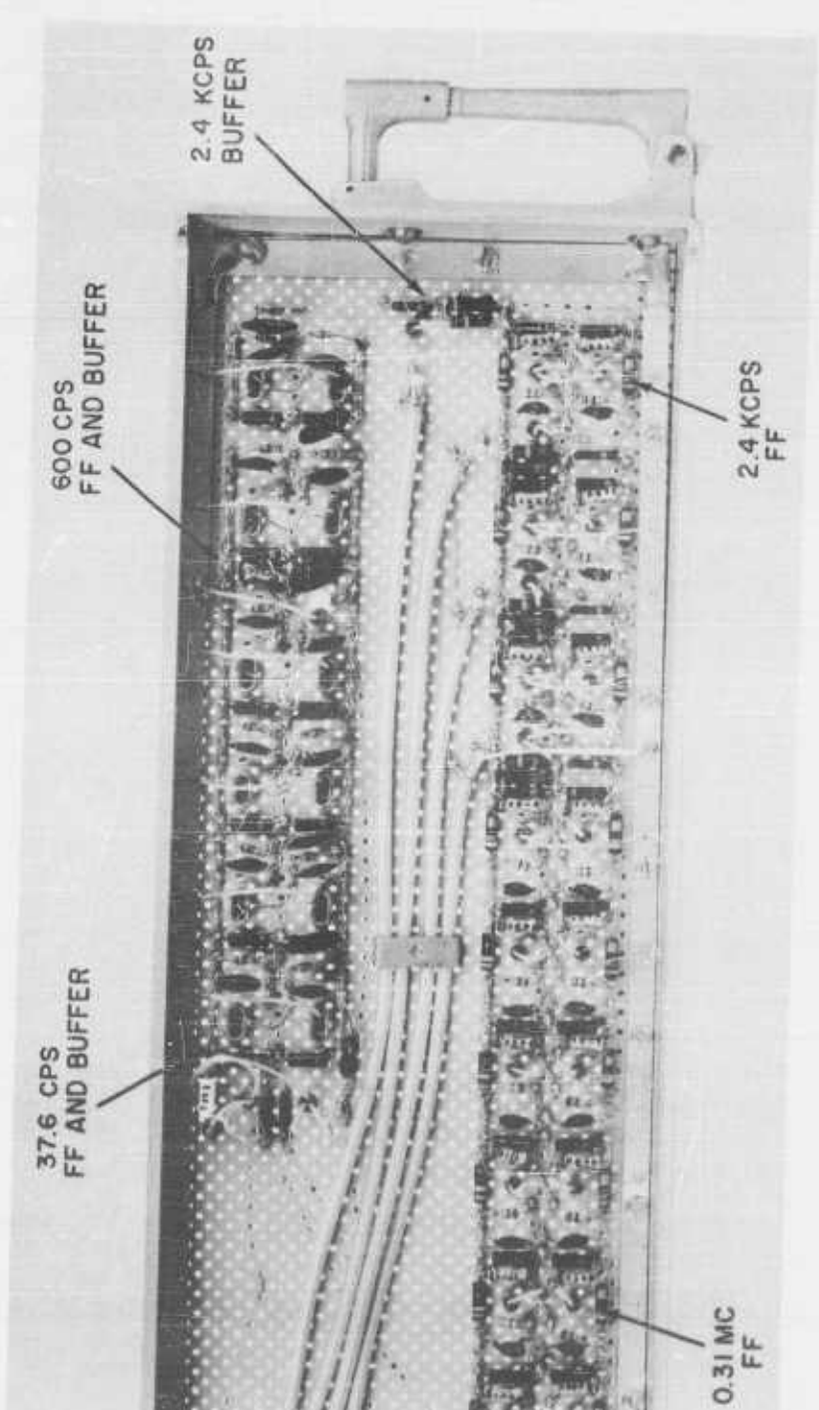


FIG. 11 POSITION COUNTER

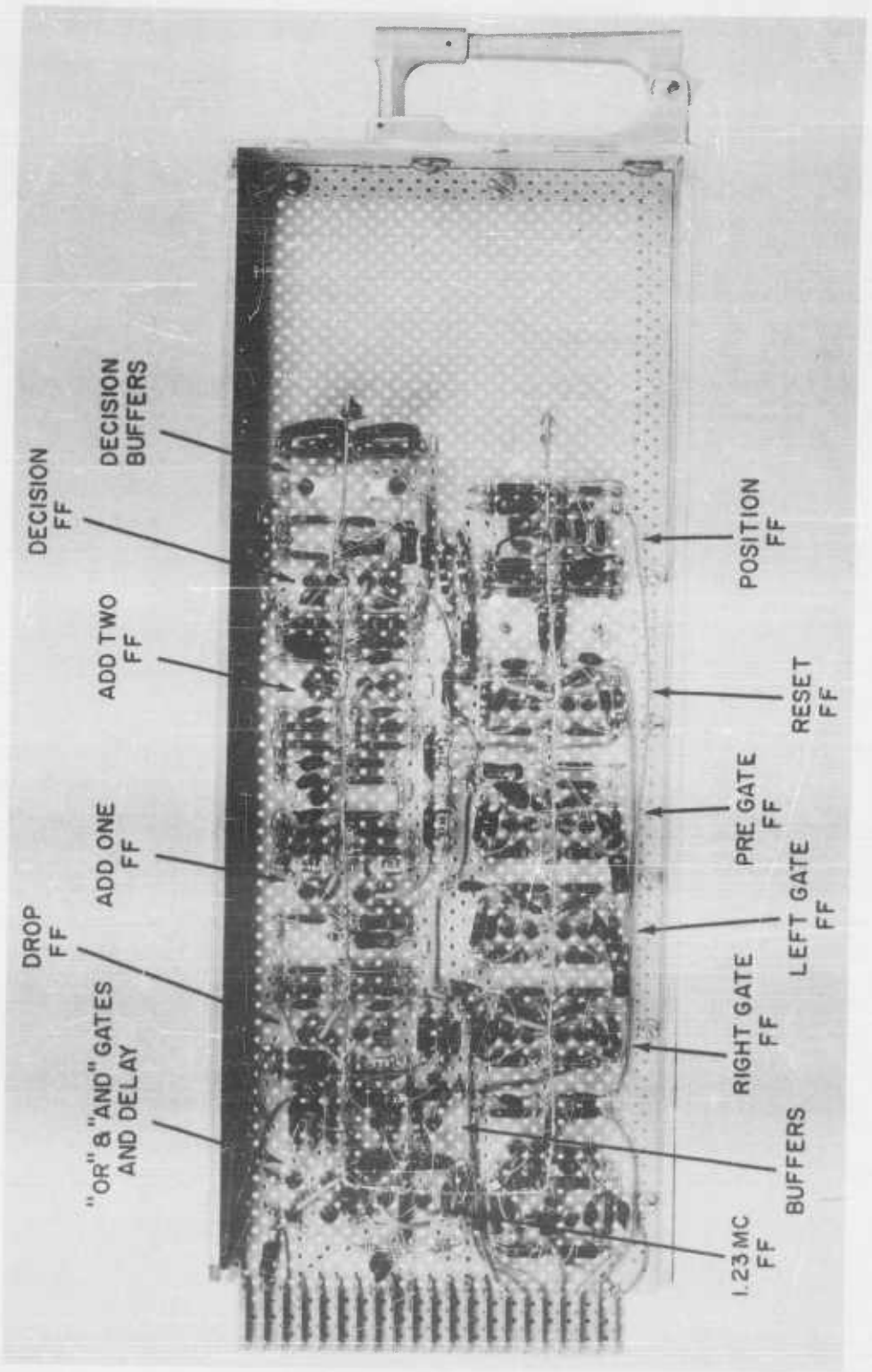


FIG. 12 POSITION CHANGING LOGIC AND GATE GENERATOR

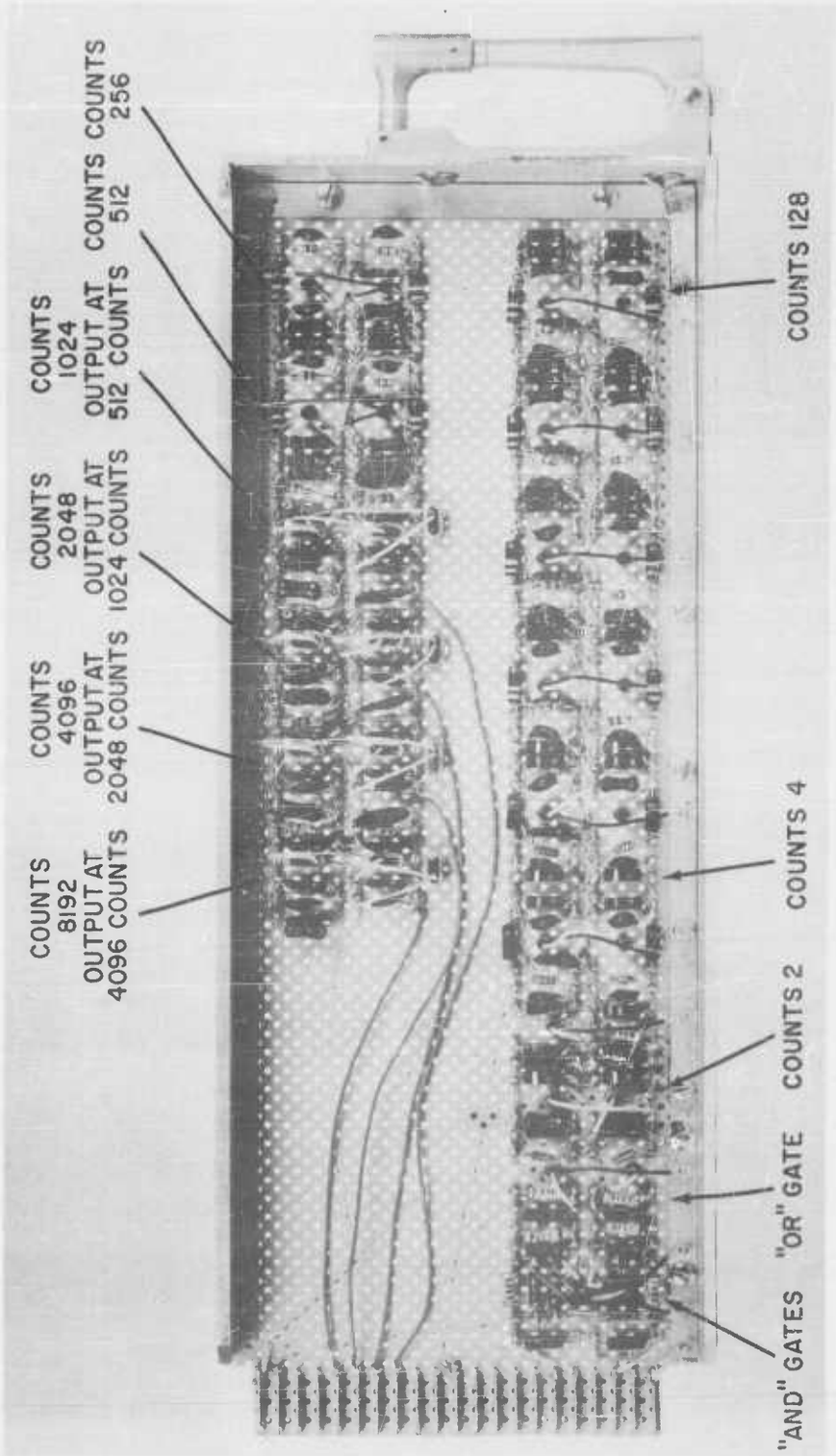


FIG. 13 DECSISION COUNTER

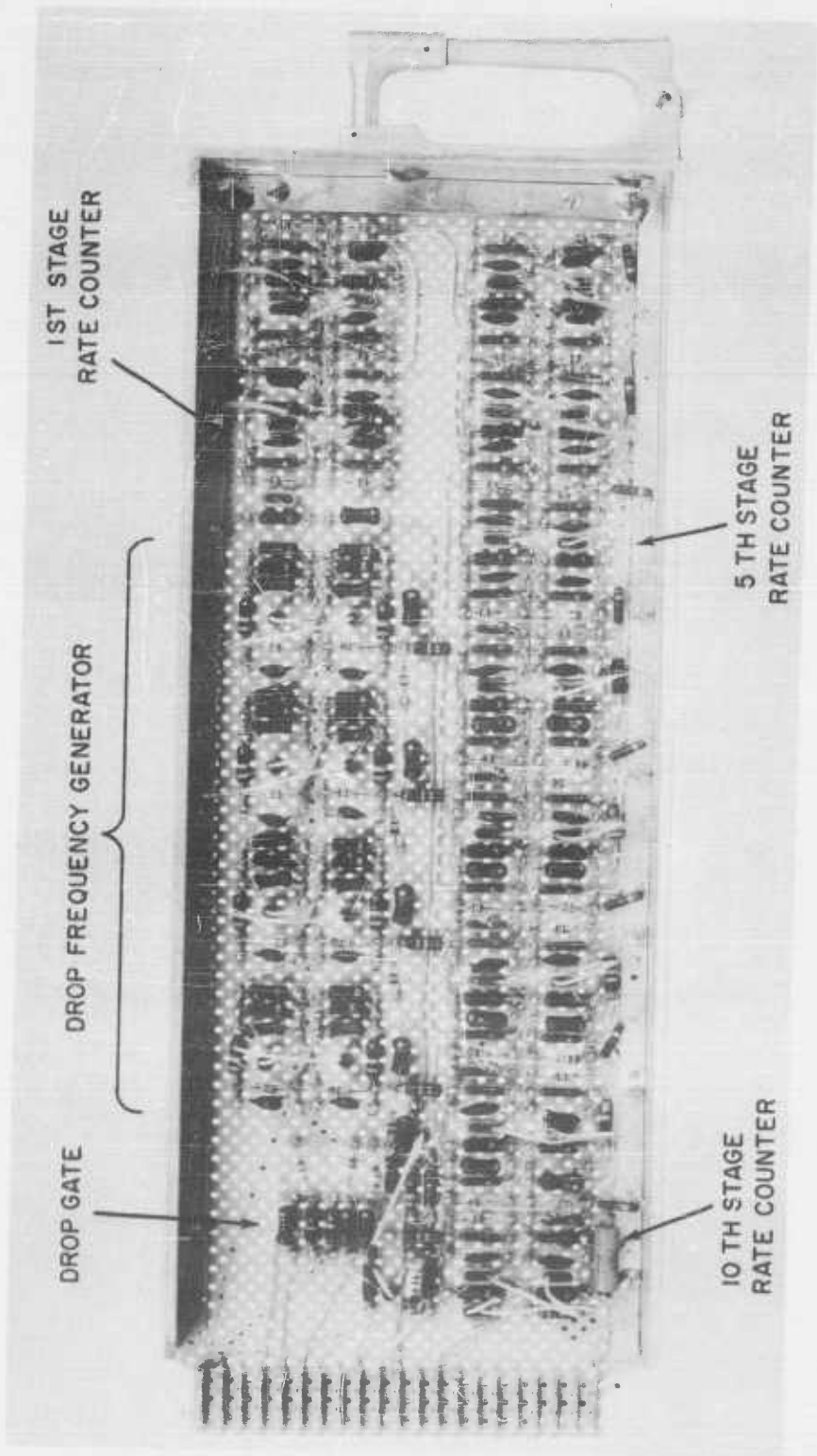


FIG. 14 RATE COUNTER AND DROP FREQUENCY GENERATOR

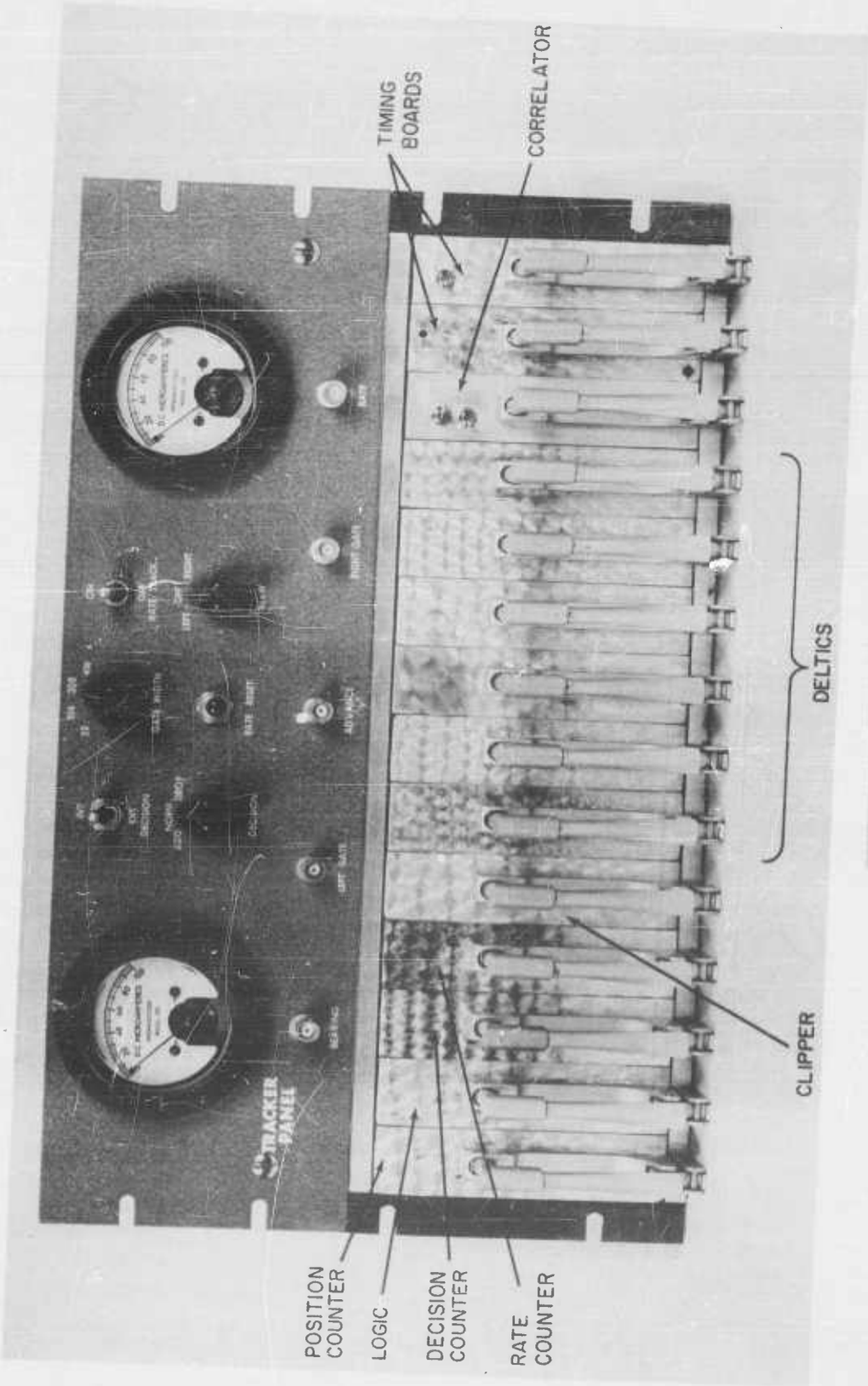


FIG. 15 FRONT PANEL AND CHASSIS

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Naval Ordnance Laboratory, White Oak, Md.
(NOL technical report 61-37)
RATE COMPENSATING TRACKER WOX-2A (U), by C.R. Greene and others. 1 June 1961. 13p. diagrs. UNCLASSIFIED

A digital automatic tracker has been built to follow a maximum of a correlation function formed by a Deltic correlator. Constant magnitude steps based on the polarity of the position error signal are taken. A rate compensating capability is included in order to track without lag correlograms moving at a constant rate.

Abstract card is unclassified

1. Trackers - WOX-2A
2. Correlators, Deltic
3. Fire control systems - Puffs

I. Title
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